Claims

What is claimed is:

1. A processor comprising cache coherency rule logic circuitry, said cache coherency rule logic circuitry to label a cache line's worth of information in accordance with at least one cache coherency rule selected from the group consisting of:

a) where said cache line's worth of information is a compressed cache line's worth of information that was written to with new information that allowed said compressed cache line's worth of information to remain compressed, keeping said compressed cache line's worth of information in the same state that it was in just prior to being written to;

b) where said cache line's worth of information is an uncompressed cache line's worth of information that was spawned from a compressed cache line's worth of information that could not remain compressed after being written to with new information, labeling said uncompressed cache line's worth of information as being in a Modified state; and,

c) where said cache line's worth of information is a compressed cache line's worth of information created by compressing an uncompressed cache line's worth of information and a companion of said uncompressed cache line's worth of information, labeling said compressed cache line's worth of information as being in a Modified state.

2. A processor comprising a hub to support said processor's participation in a multi-processor computing system that uses compressed cache lines' worth of information, said hub comprising:

a) a first bus or link interface to couple to a component of said system that can not send and receive a compressed cache line's worth of information;

b) a second bus or link interface to couple to a component of said system that can send and receive a compressed cache line's worth of information;

c) a first data path from b) to a) comprising decompression logic circuitry;

d) a second data path from b) to a) that bypasses said decompression logic circuitry;

e) a first data path from a) to b) comprising a buffer and compression logic circuitry; and,

f) a second data path from a) to b) that comprises said buffer and that bypasses said compression logic circuitry.

3. A method, comprising:

within a multi-processor computing system:

compressing a first cache line's worth of information and a second cache line's worth of information into a compressed cache line's worth of information, said first cache line's worth of information and said second cache line's worth of information being companions of one another.